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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,449	03/01/2004	Nobuaki Hashimoto	118875	9255
25944	7590	09/28/2006	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			PHAM, LONG	
			ART UNIT	PAPER NUMBER

2814

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center"><b>Advisory Action</b> <b>Before the Filing of an Appeal Brief</b></p>	<b>Application No.</b> 10/788,449	<b>Applicant(s)</b> HASHIMOTO, NOBUAKI	
	<b>Examiner</b> Long Pham	<b>Art Unit</b> 2814	

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 13 September 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
 b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
 (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
 (b) ☐ They raise the issue of new matter (see NOTE below);  
 (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
 (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
 5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
 6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
 7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
 The status of the claim(s) is (or will be) as follows:  
 Claim(s) allowed: \_\_\_\_\_.  
 Claim(s) objected to: \_\_\_\_\_.  
 Claim(s) rejected: \_\_\_\_\_.  
 Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
 9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
 10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See the attached office action.  
 12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_.  
 13. ☐ Other: \_\_\_\_\_.

Long Pham  
Primary Examiner  
Art Unit: 2814

**DETAILED ACTION**

**Advisory Action**

**Status of Amendment after final**

There are no amendments after final, the response after final dated 09/13/06 has been entered.

**Status of pending claims**

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 7, 8, 9, 10, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable Nakayama et al. (US patent 6,621,172) in combination with Hirakata et al. (US patent 6,638,781).

With respect to claims 1, 9, 10, and 18, Nakayama et al. teach an electronic device comprising (see figs. 1-6 and associated text):

A substrate 70 on which an interconnect pattern 72 is formed;

A chip component 20 having a first surface on which an electrode 22,42 is formed and a second surface opposite to the first surface, the chip component being mounted in such a manner that the second surface faces the substrate;

A section (side of chip) formed of resin and provided adjacent to the chip component; and

An interconnect 26 which is formed to extend from above the electrode, over the resin section and to above the interconnect pattern.

Nakayama et al. teach the section on the side of the chip comprises of conductive resin 74 between the chip and substrate but fail to teach that the resin is insulating.

Hirakata et al. teach that insulating resin is used because of its superior levelness and low dielectric constant. See col. 15, lines 5-15.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Hirakata into the device of Nakayama et al. to achieve the above benefit.

Further respect to claims 1 and 10, Nakayama et al. in combination with Hirakata et al. fail to teach forming a passivation layer on the first surface of the chip.

Song et al. teach forming a passivation layer on a surface of a chip to allow the formation of an electrode. See [0029].

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Song et al. into the device of Nakayama et al. and Hirakata et al. to allow the formation of electrode and subsequent interconnect.

With respect to claims 1 and 10, Nakayama et al. in combination with Hirakata et al. further teach that the insulating resin section is formed so that part of the insulating resin section does not overlay the first surface. See layer 74 of fig. 1 of Nakayama et al.

With respect to claims 7 and 16, Nakayama et al. further teach that a connection layer 74 that connects the chip component with the substrate. See figs 1-2.

With respect to claims 8 and 17, Nakayama et al. further teach that the connection layer is formed of the same material as the insulating resin section. See figs. 1 and 2.

With respect to claim 10, Nakayama et al. further teach the resin section has an inclined surface descending in an outward direction from the chip.

#### ***Response to Arguments***

Applicant's arguments filed 09/13/06 have been fully considered but they are not persuasive. See below.

In response to the applicant's arguments in the paragraphs on pages 2, 3, and 4 of the response dated 09/13/06, it is submitted that Nakayama et al. in combination with Hirakata et al. teach an insulating resin 74 having an insulating section under the wires 26 that does not overlap the first surface of the chip 20. Further, it is submitted that Nakayama et al. do not teach away from using insulating resin as an adhesive, Kakayama et al. simply teach using insulating resin as adhesive for a different reason and Hirakata et al. teach using insulating resin as an adhesive for another reason, that is to achieve superior levelness and low dielectric constant. Note that the fact that the applicants have a different reason or advantage resulting from doing what the relied prior art suggested doing is not indicative or demonstrative of unobviousness. In Re Kronig 190 USPQ 425,428 (CCPA 1976); In Re Lintner 173 USPQ 560 (CCPA 1972).

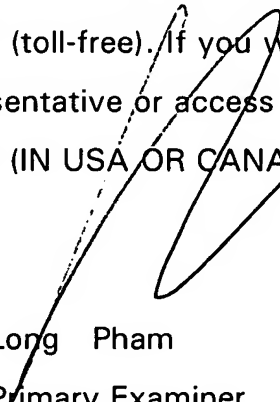
#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Long Pham  
Primary Examiner  
Art Unit 2814

LP